

# NB7L585R

## 2.5V/3.3V, 7GHz/10Gbps Differential 2:1 Mux Input to 1:6 RSECL Clock/Data Fanout Buffer / Translator

### Multi-Level Inputs w/ Internal Termination

#### Description

The NB7L585R is a differential 1:6 RSECL Clock/Data distribution chip featuring a 2:1 Clock/Data input multiplexer with an input select pin. The  $IN_x/\overline{IN}_x$  inputs incorporate internal  $50\ \Omega$  termination resistors and will accept LVPECL, CML, or LVDS logic levels.

The NB7L585R produces six identical output copies of Clock or Data operating up to 7 GHz or 10 Gb/s, respectively. As such, NB7L585R is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications.

The NB7L585R is powered with either 2.5 V or 3.3 V supply and is offered in a low profile 5mm x 5mm 32-pin QFN package.

Application notes, models, and support documentation are available at [www.onsemi.com](http://www.onsemi.com).

The NB7L585R is a member of the GigaComm™ family of high performance clock products.

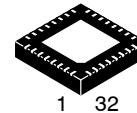
#### Features

- Maximum Input Data Rate > 10 Gb/s Typical
- Data Dependent Jitter < 10 ps
- Maximum Input Clock Frequency > 7 GHz Typical
- Random Clock Jitter < 0.8 ps RMS
- Low Skew 1:6 RSECL Outputs, 20 ps max
- 2:1 Multi-Level Mux Inputs
- 160 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- Differential RSECL Outputs, 400 mV peak-to-peak, typical
- Operating Range:  $V_{CC} = 2.375\text{ V to }3.6\text{ V}$  with  $GND = 0\text{ V}$
- Internal  $50\ \Omega$  Input Termination Resistors
- VREFAC Reference Output
- QFN-32 Package, 5mm x 5mm
- $-40^\circ\text{C to }+85^\circ\text{C}$  Ambient Operating Temperature
- These Devices are Pb-Free and are RoHS Compliant



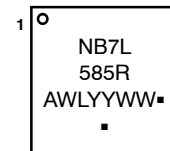
ON Semiconductor®

<http://onsemi.com>



**QFN32**  
**MN SUFFIX**  
**CASE 488AM**

#### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

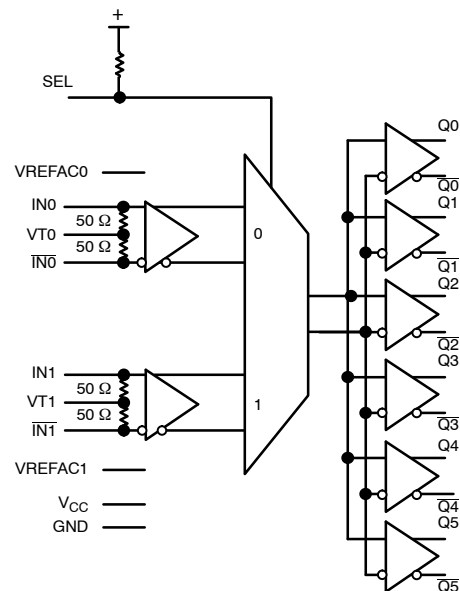


Figure 1. Simplified Block Diagram

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

# NB7L585R

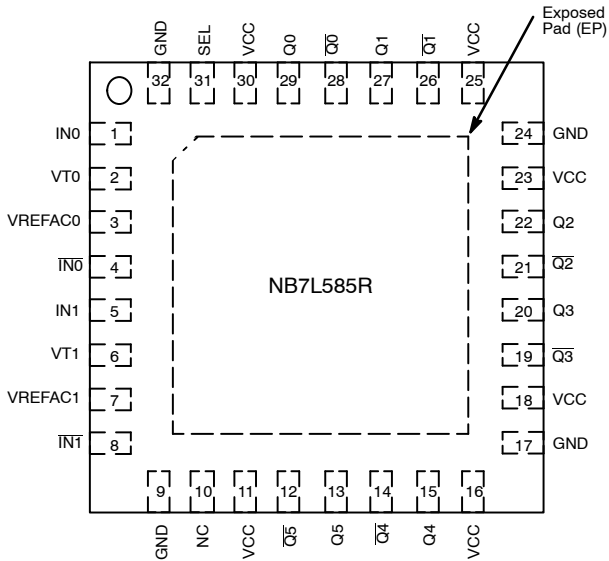


Figure 2. Pinout: QFN-32 (Top View)

Table 1. INPUT SELECT FUNCTION TABLE

SEL*	CLK Input Selected
0	IN0
1	IN1

\*Defaults HIGH when left open.

Table 2. PIN DESCRIPTION

Pin Number	Pin Name	I/O	Pin Description
1,4 5,8	IN0, $\overline{\text{IN0}}$ IN1, $\overline{\text{IN1}}$	LVPECL, CML, LVDS Input	Non-inverted, Inverted, Differential Data Inputs internally biased to $V_{CC}/2$
2,6	VT0, VT1		Internal 100 $\Omega$ Center-tapped Termination Pin for IN0 / $\overline{\text{IN0}}$ and IN1 / $\overline{\text{IN1}}$
31	SEL	LVTTTL/LVCMOS Input	Input Select pin; LOW for IN0 Inputs, HIGH for IN1 Inputs; defaults HIGH when left open
10	NC	-	No Connect
11, 16, 18 23, 25, 30	$V_{CC}$	-	Positive Supply Voltage. All $V_{CC}$ pins must be connected to the positive power supply for correct DC and AC operation.
29, 28 27, 26 22, 21 20, 19 15, 14 13, 12	Q0, $\overline{\text{Q0}}$ Q1, $\overline{\text{Q1}}$ Q2, $\overline{\text{Q2}}$ Q3, $\overline{\text{Q3}}$ Q4, $\overline{\text{Q4}}$ Q5, $\overline{\text{Q5}}$	RSECL Output	Non-inverted, Inverted Differential Outputs Note 1.
9, 17, 24, 32	GND		Negative Supply Voltage, connected to Ground
3 7	VREFAC0 VREFAC1	-	Output Voltage Reference for Capacitor-Coupled Inputs
-	EP	-	The Exposed Pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pins (VT0, VT1) are connected to a common termination voltage or left open, and if no signal is applied on INn/ $\overline{\text{INn}}$  input, then the device will be susceptible to self-oscillation.
2. All  $V_{CC}$  and GND pins must be externally connected to a power supply for proper operation.

# NB7L585R

**Table 3. ATTRIBUTES**

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
R <sub>PU</sub> – SEL Input Pullup Resistor		37.5 kΩ
Moisture Sensitivity (Note 3)	QFN–32	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in
Transistor Count		303
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		+4.0	V
V <sub>IO</sub>	Input/Output Voltage	GND = 0 V		–0.5 to V <sub>CC</sub> +0.5	V
V <sub>INPP</sub>	Differential Input Voltage  I <sub>N</sub> – I <sub>N</sub>			1.89	V
I <sub>IN</sub>	Input Current Through R <sub>T</sub> (50 Ω Resistor)			± 40	mA
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA
I <sub>VREFAC</sub>	VREFAC Sink or Source Current			± 1.5	mA
T <sub>A</sub>	Operating Temperature Range			–40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			–65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction–to–Ambient) (Note 4)	0 lfpm 500 lfpm	QFN32 QFN32	31 27	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction–to–Case) (Note 4)		QFN32	12	°C/W
T <sub>sol</sub>	Wave Solder			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

# NB7L585R

**Table 5. DC CHARACTERISTICS POSITIVE RSECL OUTPUT**  $V_{CC} = 2.375\text{ V to }3.6\text{ V}$ ;  $GND = 0\text{ V}$ ;  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
<b>POWER SUPPLY</b>					
$V_{CC}$	Power Supply Voltage $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	3.0 2.375	3.3 2.5	3.6 2.625	V
$I_{CC}$	Power Supply Current (Inputs and Outputs Open)		185	225	mA
<b>RSECL Outputs</b>					
$V_{OH}$	Output HIGH Voltage (Note 6) $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1300$ 2000 1200	$V_{CC} - 1125$ 2175 1375	$V_{CC} - 1000$ 2300 1500	mV
$V_{OL}$	Output LOW Voltage (Note 6) $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1800$ 1500 700	$V_{CC} - 1525$ 1775 975	$V_{CC} - 1350$ 1950 1150	mV
<b>DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED</b> (Note 7) (Figures 5 & 6)					
$V_{IH}$	Single-ended Input HIGH Voltage	$V_{th} + 100$		$V_{CC}$	mV
$V_{IL}$	Single-ended Input LOW Voltage	GND		$V_{th} - 100$	mV
$V_{th}$	Input Threshold Reference Voltage Range (Note 8)	1100		$V_{CC} - 100$	mV
$V_{ISE}$	Single-ended Input Voltage ( $V_{IH} - V_{IL}$ )	200		$V_{CC} - GND$	mV
<b>VREFACx</b> (for Capacitor- Coupled Inputs, Only)					
$V_{REFAC}$	Output Reference Voltage @100 $\mu\text{A}$ for Capacitor- Coupled Inputs, Only	$V_{CC} - 1350$	$V_{CC} - 1150$	$V_{CC} - 1000$	mV
<b>DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY</b> (Figures 7 & 8) (Note 9)					
$V_{IHD}$	Differential Input HIGH Voltage ( $I_N, \bar{I}_N$ )	1200		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage ( $I_N, \bar{I}_N$ )	GND		$V_{IHD} - 100$	mV
$V_{ID}$	Differential Input Voltage ( $I_N, \bar{I}_N$ ) ( $V_{IHD} - V_{ILD}$ )	100		1200	mV
$V_{CMR}$	Input Common Mode Range (Differential Configuration, Note 10) (Figure 9)	1050		$V_{CC} - 50$	mV
$I_{IH}$	Input HIGH Current $I_N/\bar{I}_N$ ( $V_{TIN}/\bar{V}_{TIN}$ Open)	-150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current $I_N/\bar{I}_N$ ( $V_{TIN}/\bar{V}_{TIN}$ Open)	-150		150	$\mu\text{A}$
<b>CONTROL INPUT (SEL Pin)</b>					
$V_{IH}$	Input HIGH Voltage for Control Pin	2.0		$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage for Control Pin	GND		0.8	mV
$I_{IH}$	Input HIGH Current	-150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150		150	$\mu\text{A}$
<b>TERMINATION RESISTORS</b>					
$R_{TIN}$	Internal Input Termination Resistor (Measured from $I_N$ x to $V_{T_x}$ )	45	50	55	$\Omega$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .
- RSECL outputs ( $Q_n/\bar{Q}_n$ ) loaded with 50  $\Omega$  to  $V_{CC} - 2\text{ V}$  for proper operation.
- $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.
- $V_{th}$  is applied to the complementary input when operating in single-ended mode.
- $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{CMR}$  parameters must be complied with simultaneously.
- $V_{CMR}$  min varies 1:1 with GND,  $V_{CMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{CMR}$  range is referenced to the most positive side of the differential input signal.

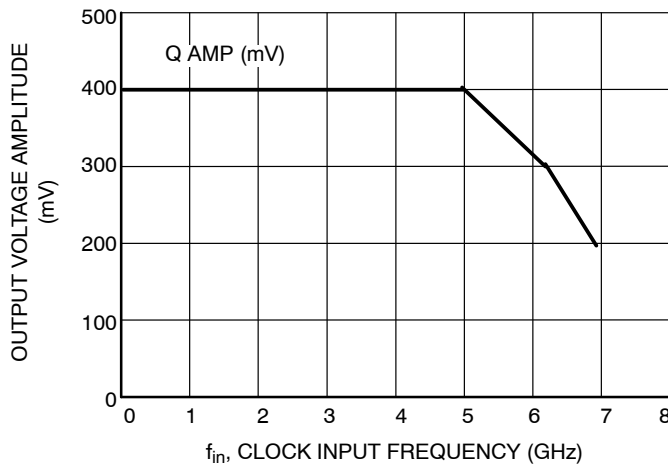
# NB7L585R

**Table 6. AC CHARACTERISTICS**  $V_{CC} = 2.375\text{ V to }3.6\text{ V}$ ;  $GND = 0\text{ V}$ ;  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (Note 11)

Symbol	Characteristic	Min	Typ	Max	Unit
$f_{MAX}$	Maximum Input Clock Frequency; $V_{OUTpp} \geq 200\text{ mV}$	6	7		GHz
$f_{DATAMAX}$	Maximum Operating Data Rate (PRBS23)	8	10		Gbps
$f_{SEL}$	Maximum Toggle Frequency, SEL	1.0	1.5		GHz
$V_{OUTpp}$	Output Voltage Amplitude (@ $V_{INPPmin}$ ) (Note 12) (Figures 8 and 10)				mV
		$f_{in} \leq 6.0\text{ GHz}$			
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Differential Outputs, @ 1 GHz, measured at differential crosspoint				ps
		IN/ $\bar{I}$ N to Q/ $\bar{Q}$ SEL to Q		100 160 200 225 300	
$t_{PLH\ TC}$	Propagation Delay Temperature Coefficient		50		$\Delta fs/^\circ C$
tskew	Output – Output skew (within device) (Note 13) Device – Device skew (tpd max – tpdmin)			20 100	ps
$t_{DC}$	Output Clock Duty Cycle (Reference Duty Cycle = 50%)				%
		$f_{in} \leq 6.0\text{ GHz}$		45 50 55	
$\Phi_N$	Phase Noise, $f_c = 1\text{ GHz}$				dBc
		10 kHz	-134		
		100 kHz	-136		
		1 MHz	-149		
		10 MHz	-150		
		20 MHz	-150		
		40 MHz	-151		
$t_{f\Phi N}$	Integrated Phase Jitter (Figure x) $f_c = 1\text{ GHz}$ , 12 kHz – 20 MHz Offset (RMS)		36		fs
$t_{JITTER}$	RJ – Output Random Jitter (Note 14) DJ – Residual Output Deterministic Jitter (Note 15)				ps RMS ps pk-pk
		$f_{in} \leq 5.0\text{ GHz}$ $\leq 8\text{ Gbps}$		0.2 2.0	0.8 10
	Crosstalk Induced Jitter (Adjacent Channel) (Note 17)			0.7	ps RMS
$V_{INPP}$	Input Voltage Swing (Differential Configuration) (Note 16)	100		1200	mV
$t_r, t_f$	Output Rise/Fall Times @ 1 GHz (20% – 80%), Q, $\bar{Q}$	15	40	70	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured using a 400 mV pk-pk source, 50% duty cycle clock source. All output loading with external  $50\ \Omega$  to  $V_{CC} - 2\text{ V}$ . Input edge rates 40 ps (20% – 80%).
12. Output voltage swing is a single-ended measurement operating in differential mode.
13. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross-point of the inputs to the crosspoint of the outputs.
14. Additive RMS jitter with 50% duty cycle clock signal.
15. Additive Peak-to-Peak data dependent jitter with input NRZ data at PRBS23.
16. Input voltage swing is a single-ended measurement operating in differential mode.
17. Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.



**Figure 3. Clock Output Voltage Amplitude ( $V_{OUTpp}$ ) vs. Input Frequency ( $f_{in}$ ) at Ambient Temperature (Typical)**

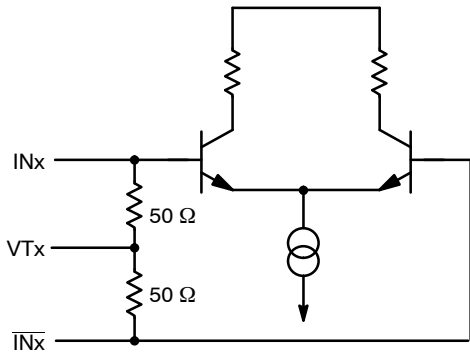


Figure 4. Input Structure

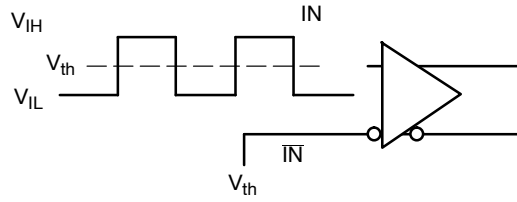


Figure 5. Differential Input Driven Single-Ended

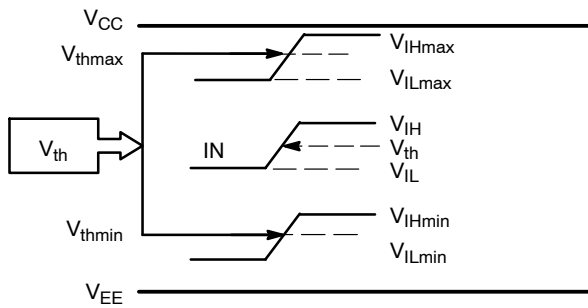


Figure 6.  $V_{th}$  Diagram

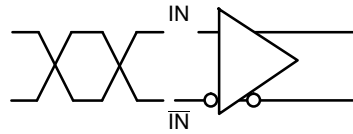


Figure 7. Differential Inputs Driven Differentially

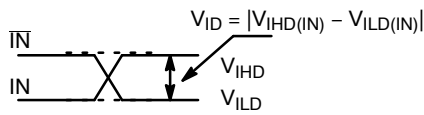


Figure 8. Differential Inputs Driven Differentially

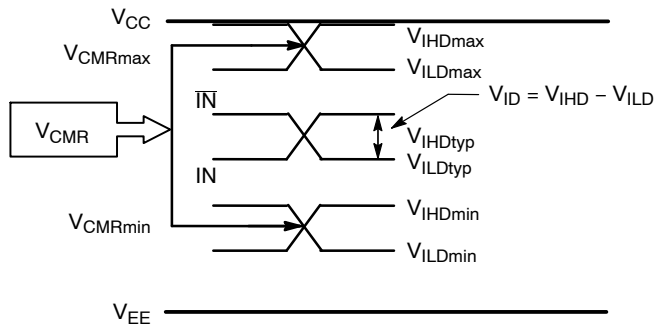


Figure 9. VCMR Diagram

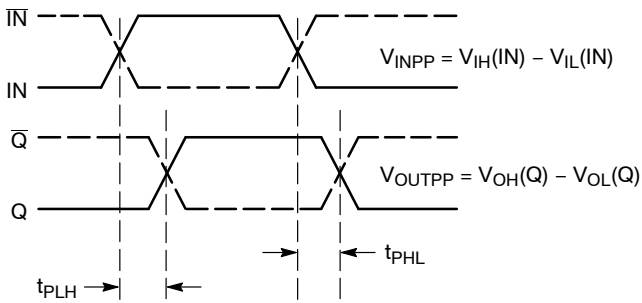


Figure 10. AC Reference Measurement

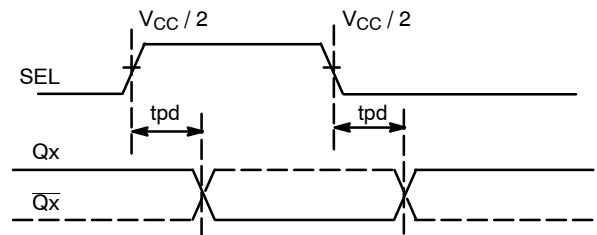


Figure 11. SEL to Qx Timing Diagram

# NB7L585R

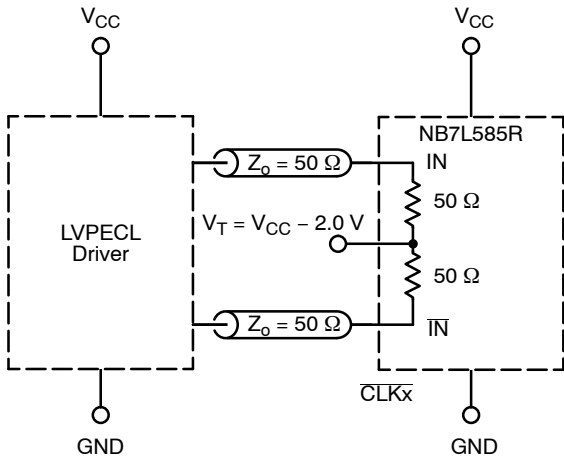


Figure 12. LVPECL Interface

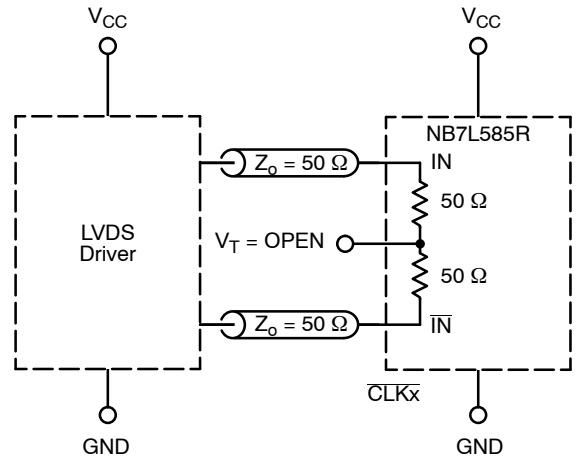


Figure 13. LVDS Interface

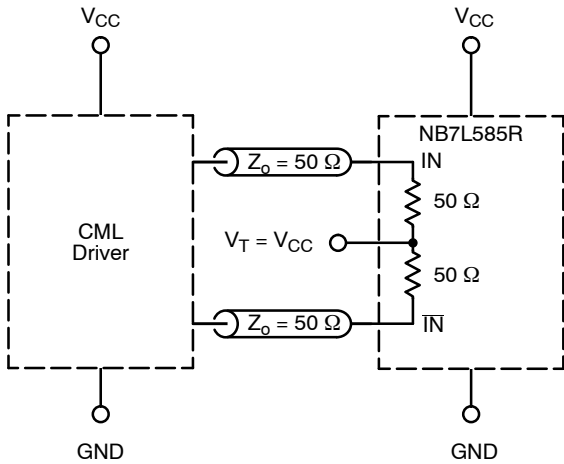


Figure 14. Standard 50  $\Omega$  Load CML Interface

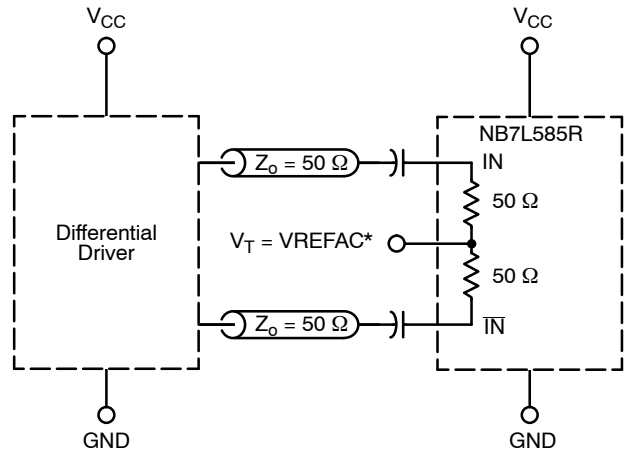


Figure 15. Capacitor-Coupled Differential Interface ( $V_T$  Connected to  $V_{REFAC}$ )

\* $V_{REFAC}$  bypassed to ground with a 0.01  $\mu F$  capacitor.

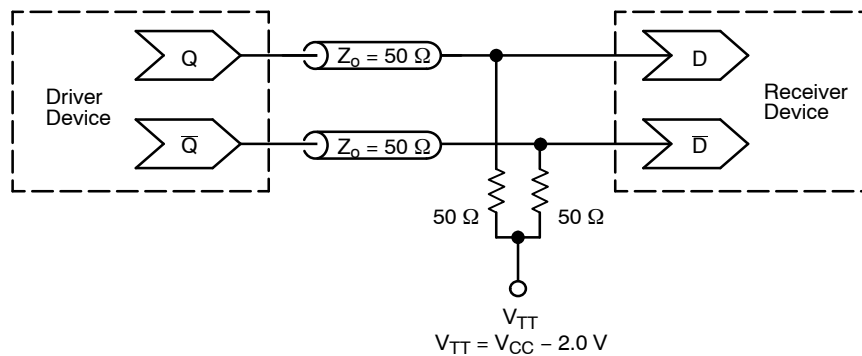


Figure 16. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

# NB7L585R

## DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NB7L585RMNG	QFN-32 (Pb-Free)	74 Units / Rail
NB7L585RMNR4G	QFN-32 (Pb-Free)	1000 / Tape & Reel

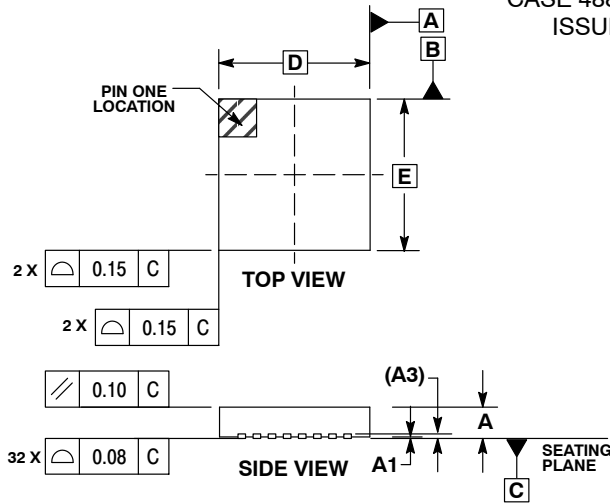
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



# NB7L585R

## PACKAGE DIMENSIONS

QFN32 5\*5\*1 0.5 P  
CASE 488AM-01  
ISSUE O

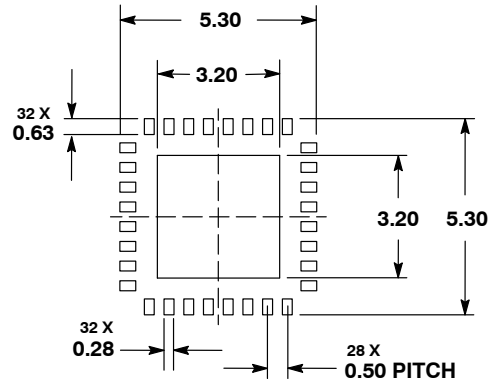


**NOTES:**

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3	0.200 REF		
b	0.180	0.250	0.300
D	5.00 BSC		
D2	2.950	3.100	3.250
E	5.00 BSC		
E2	2.950	3.100	3.250
e	0.500 BSC		
K	0.200	---	---
L	0.300	0.400	0.500

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GigaComm is a trademark of Semiconductor Component Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative